

FIG. 1

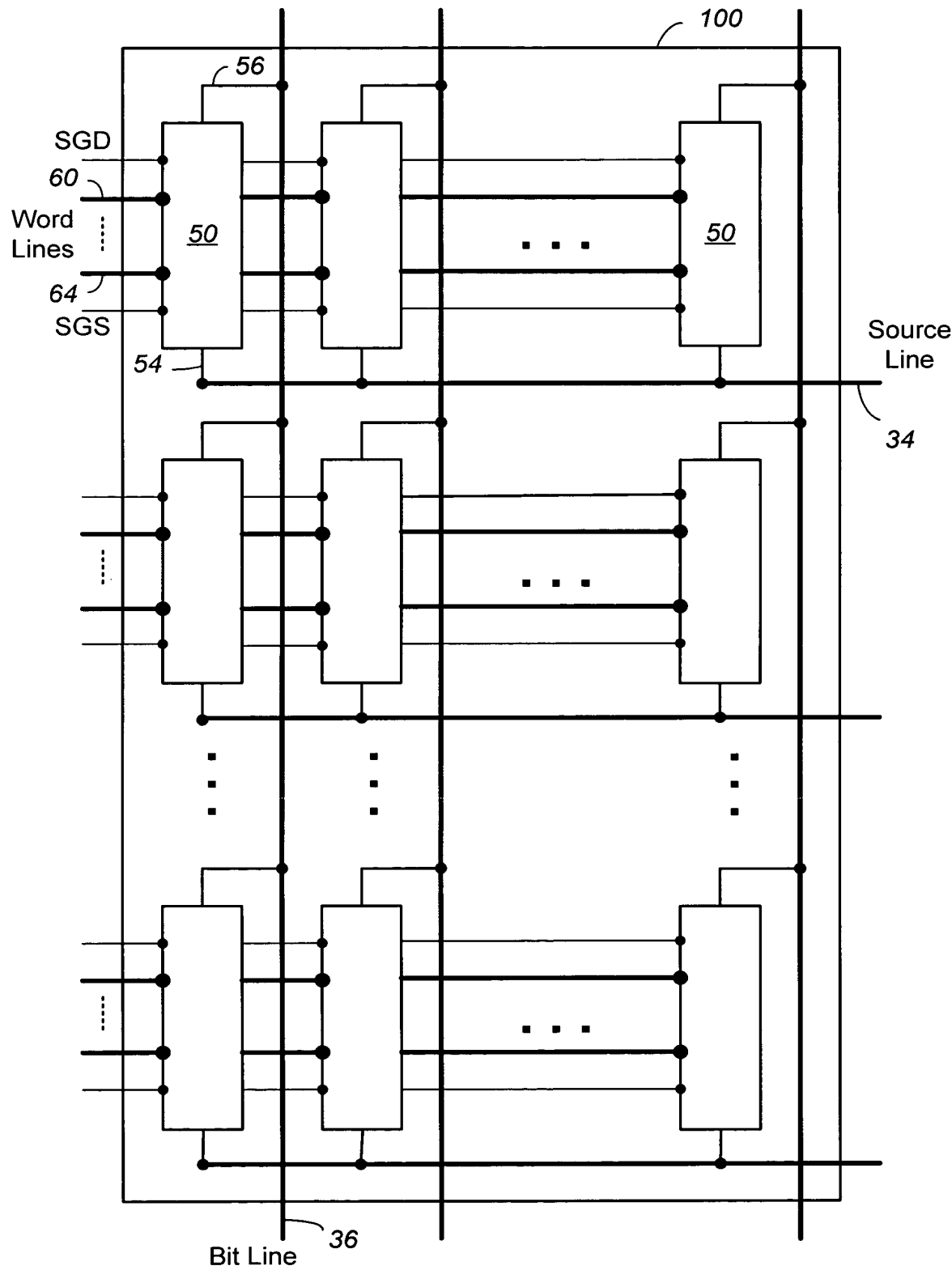


FIG. 3

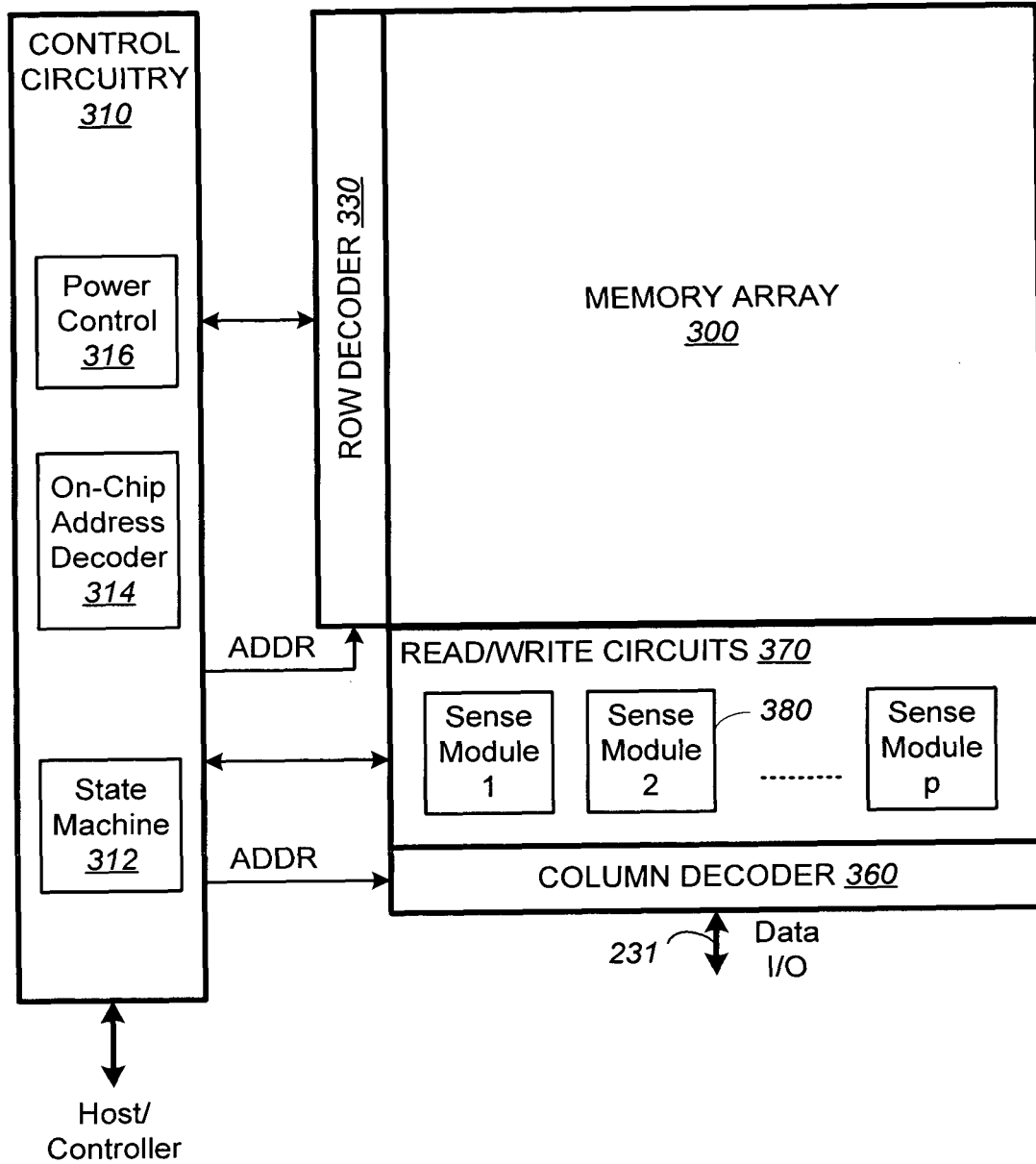


FIG. 4A

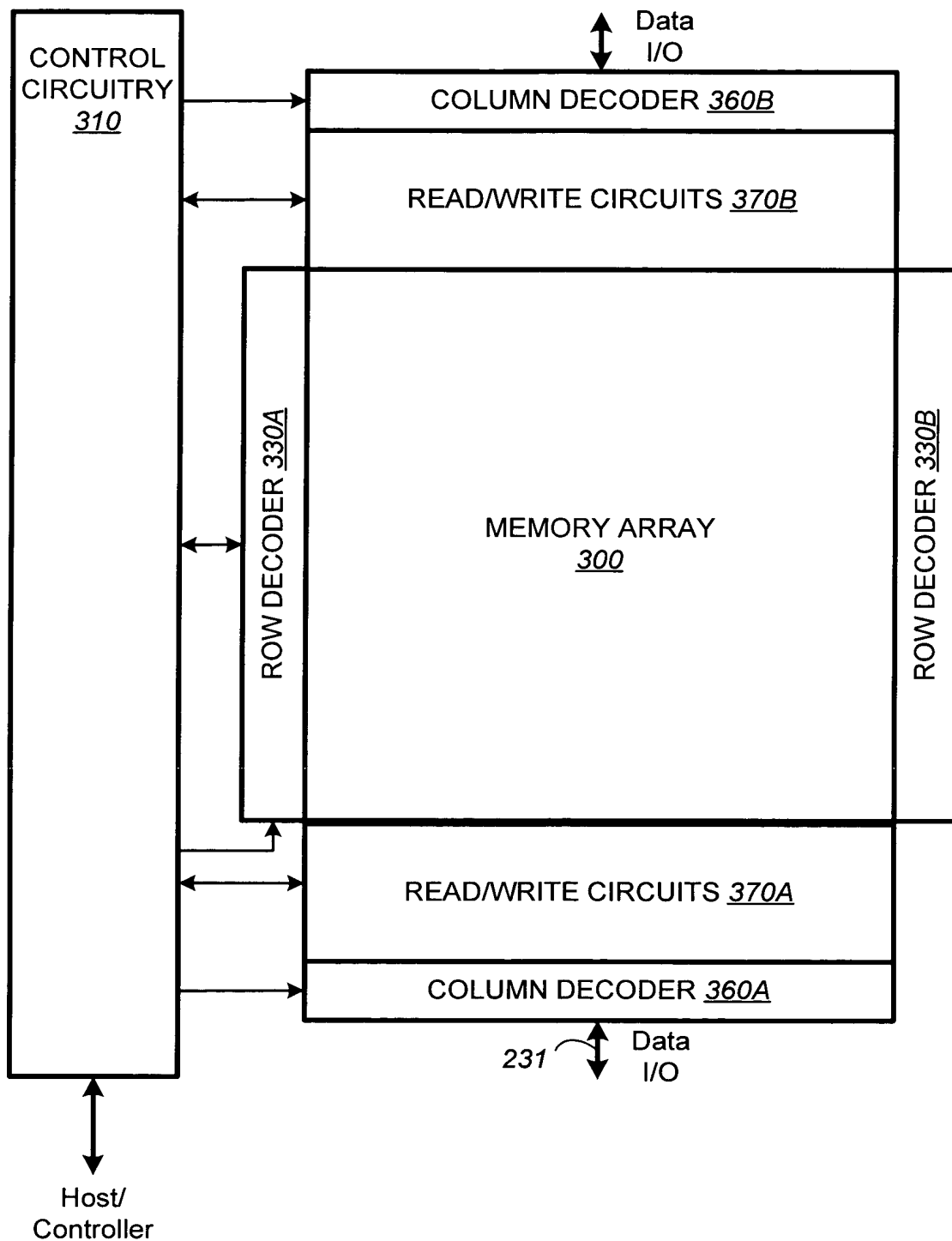


FIG. 4B

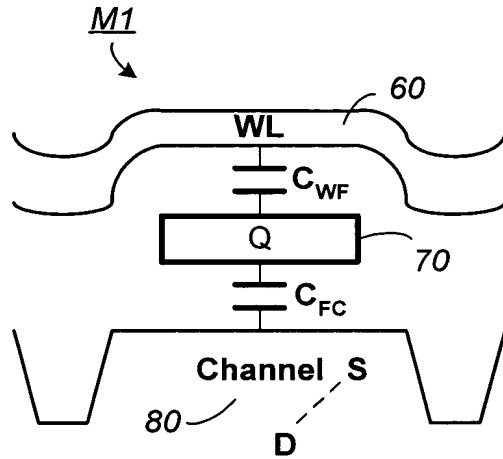


FIG. 5A

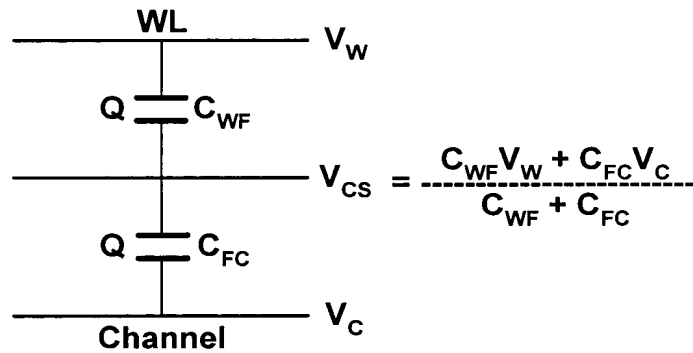


FIG. 5B

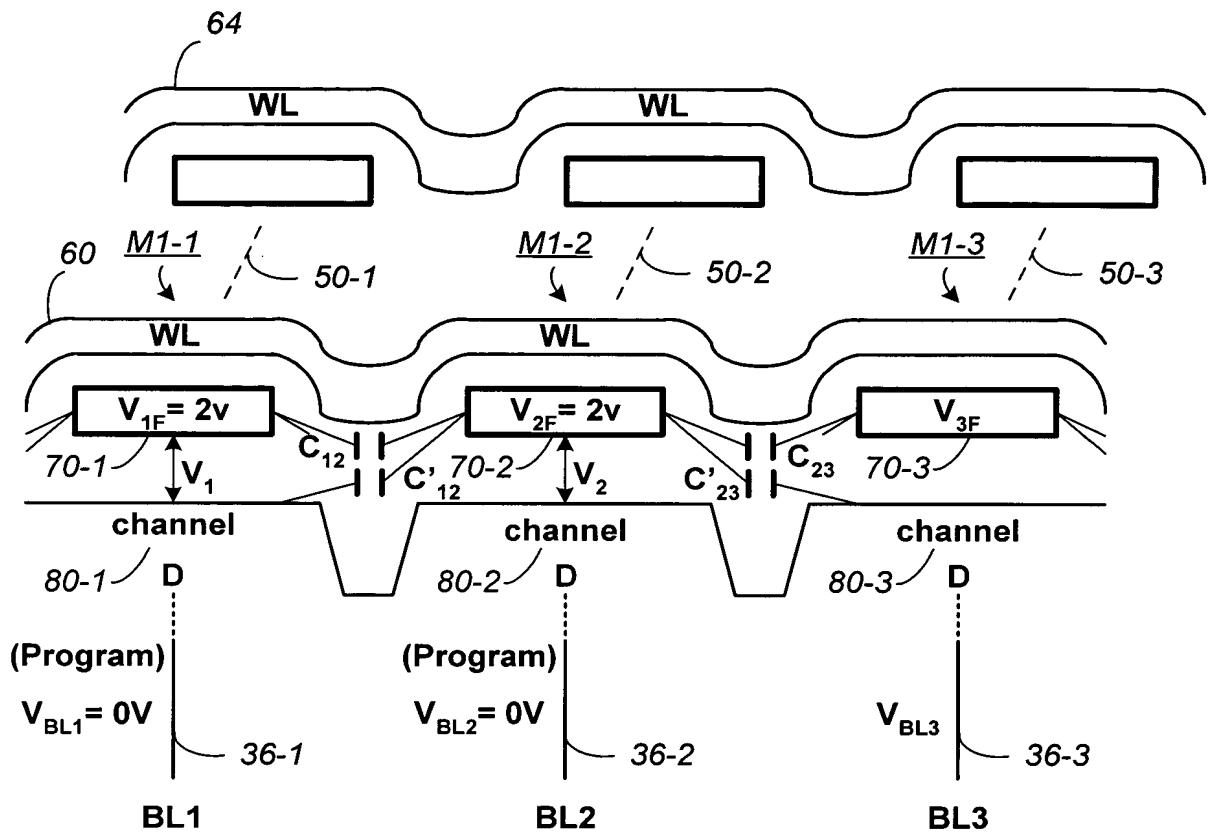


FIG. 6A

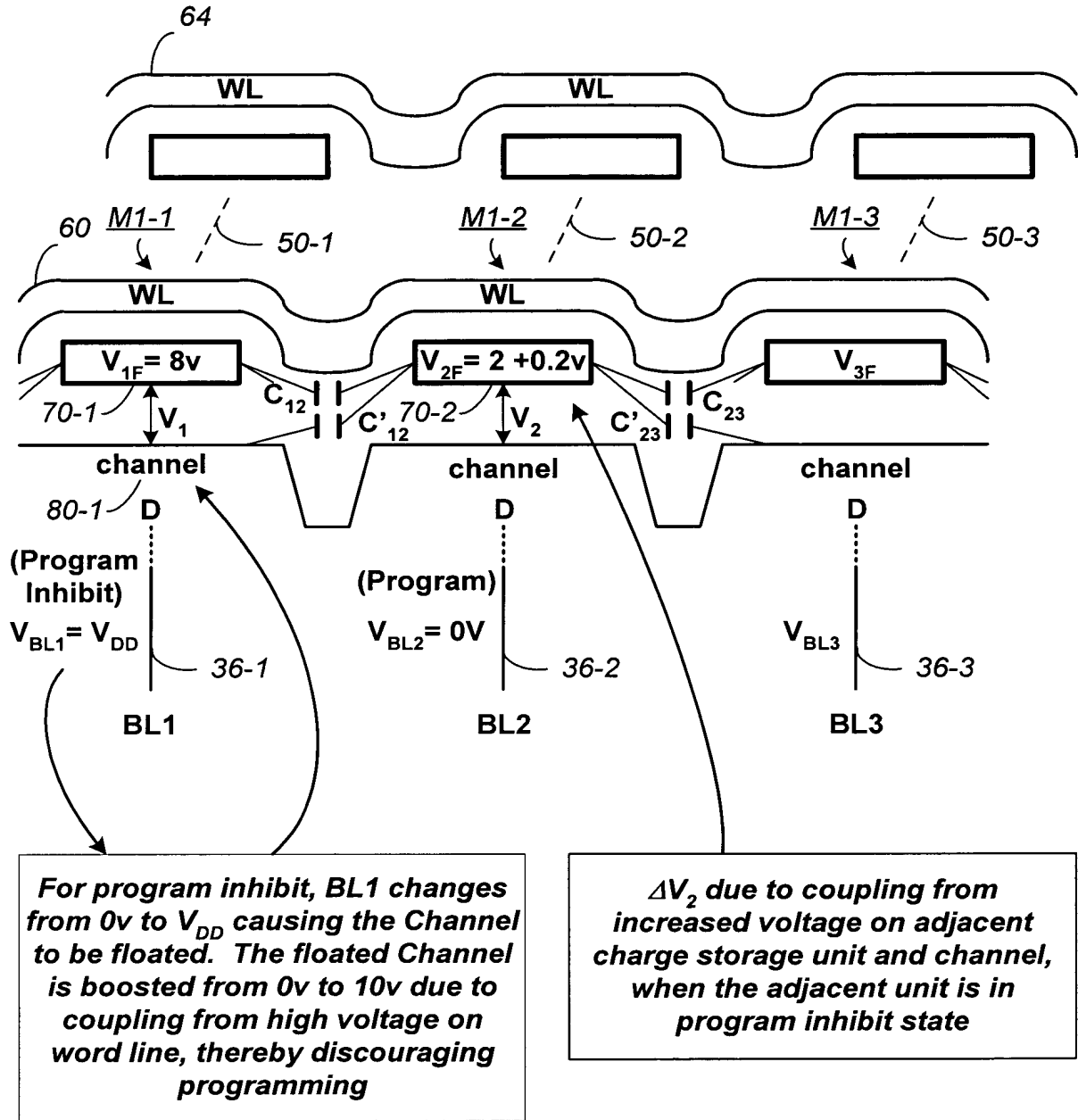


FIG. 6B

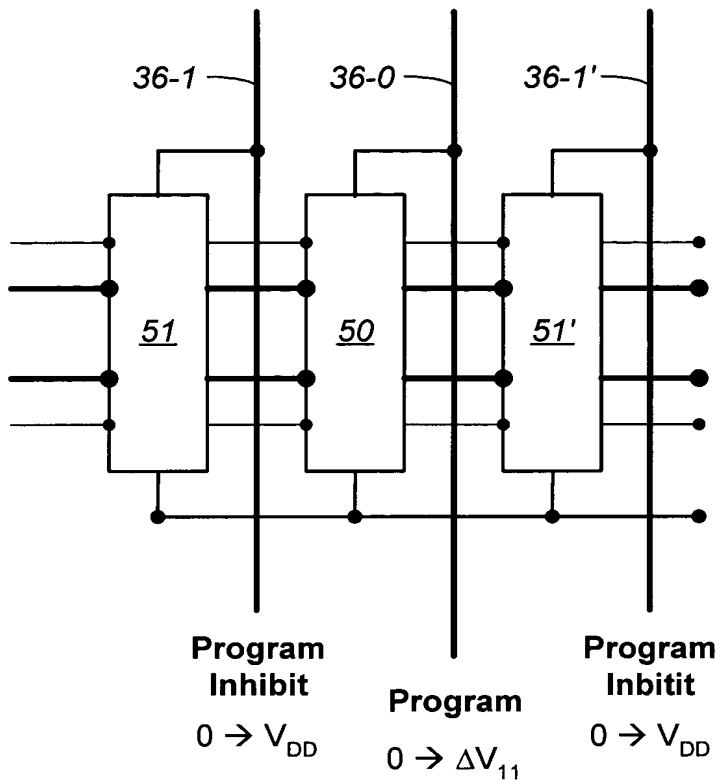


FIG. 7A

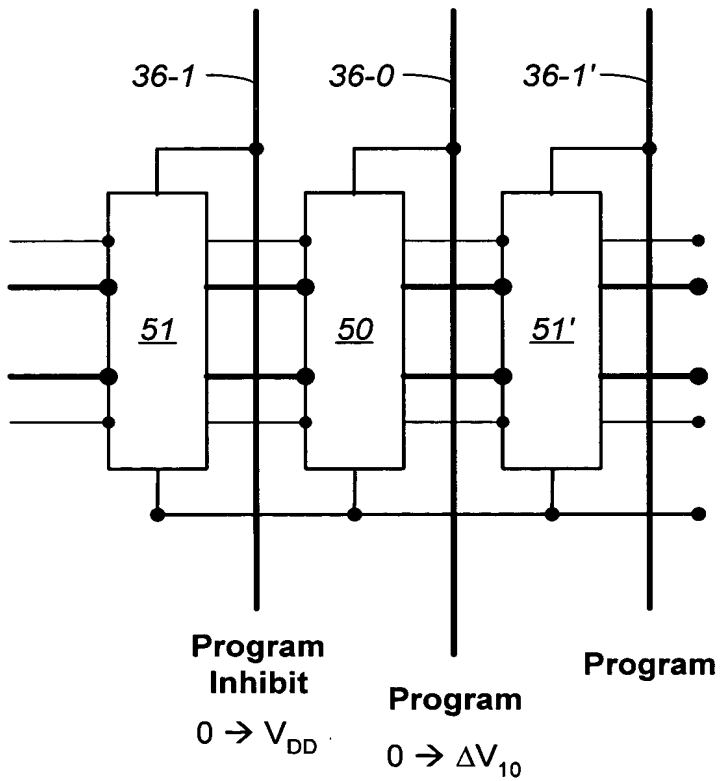


FIG. 7B

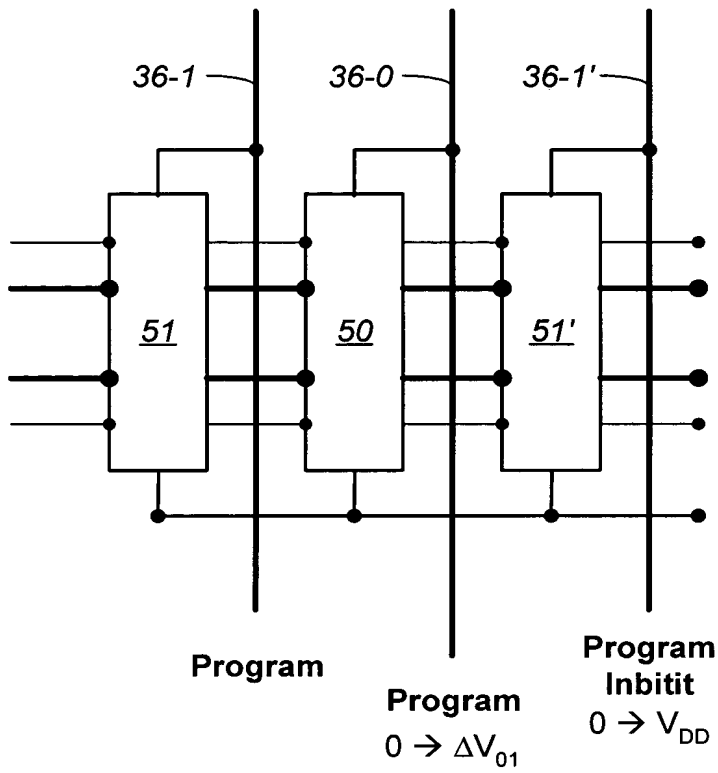


FIG. 7C

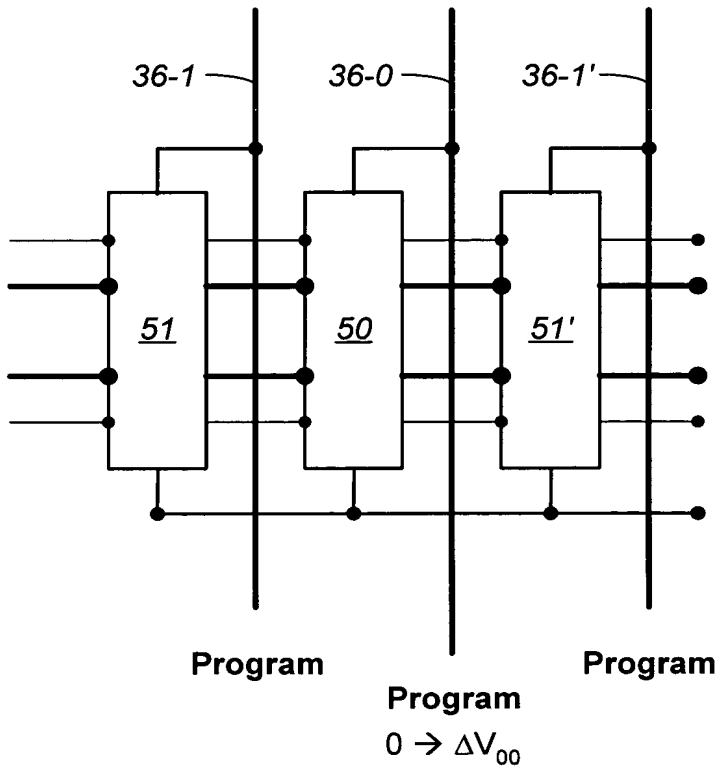


FIG. 7D

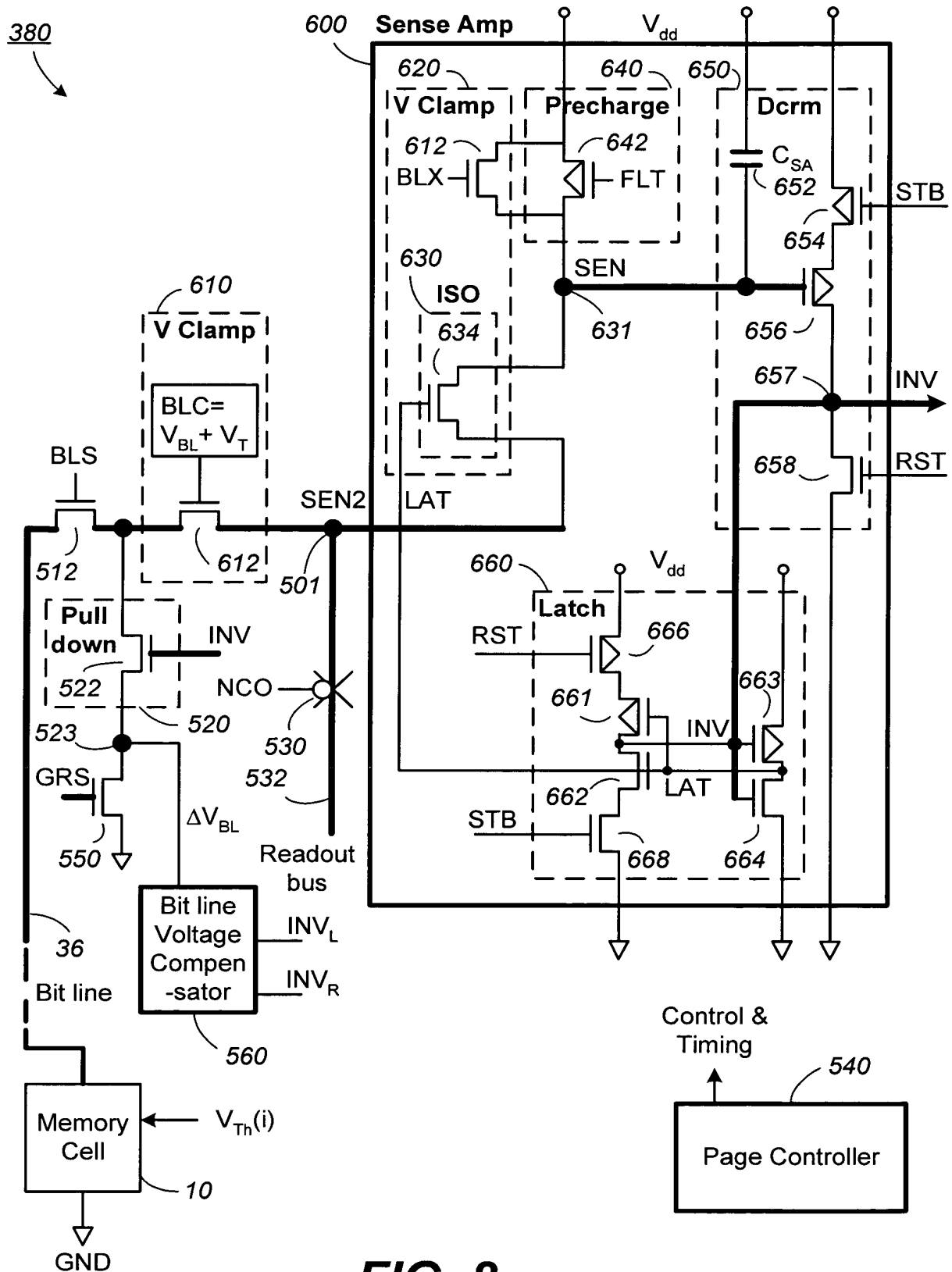


FIG. 8

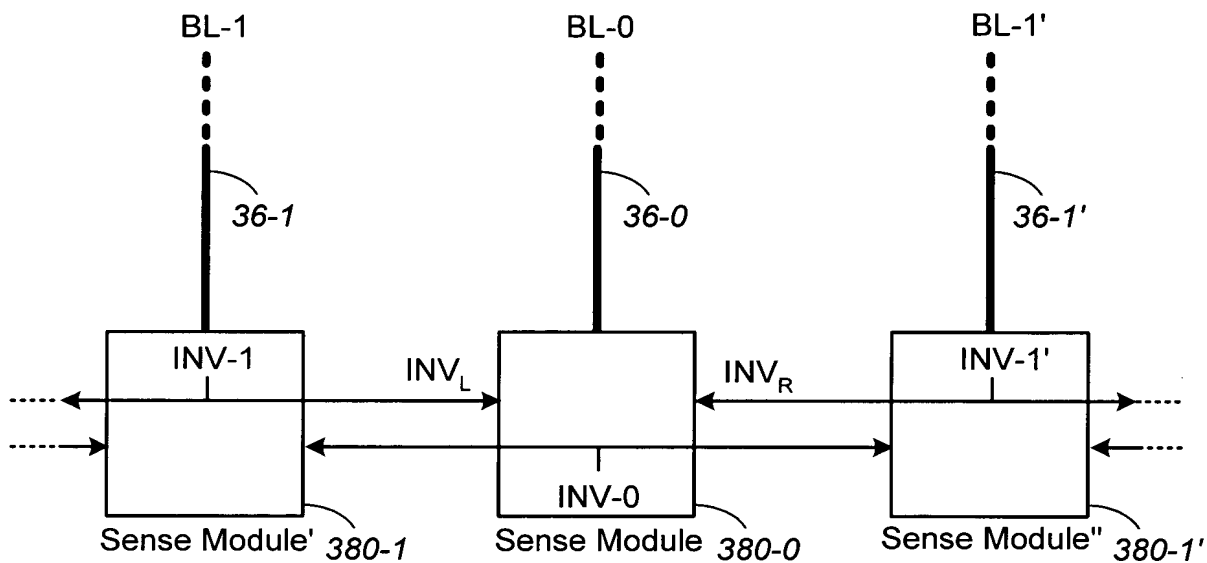


FIG. 9

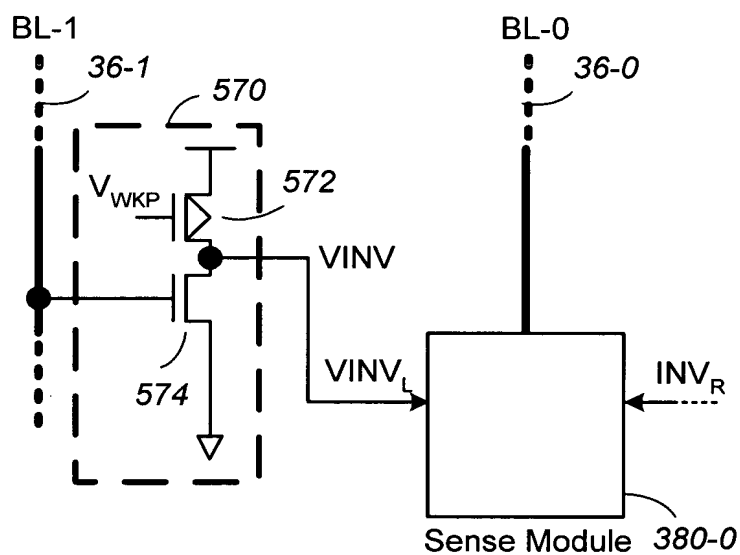


FIG. 10

LEFT NEIGHBOR			Programming Storage Unit	RIGHT NEIGHBOR		
MODE	INV _L	V _{BL-1}	Bit line Offset ΔV_{BL-0}	MODE	INV _R	V _{BL-1'}
Program Inhibit	LOW	V _{DD}	ΔV_{11} (e.g., 0.3V)	Program Inhibit	LOW	V _{DD}
Program Inhibit	LOW	V _{DD}	ΔV_{10} (e.g., 0.15V)	Program	HIGH	ΔV
Program	HIGH	ΔV	ΔV_{01} (e.g., 0.15V)	Program Inhibit	LOW	V _{DD}
Program	HIGH	ΔV	ΔV_{00} (e.g., 0V)	Program	HIGH	ΔV

FIG. 11

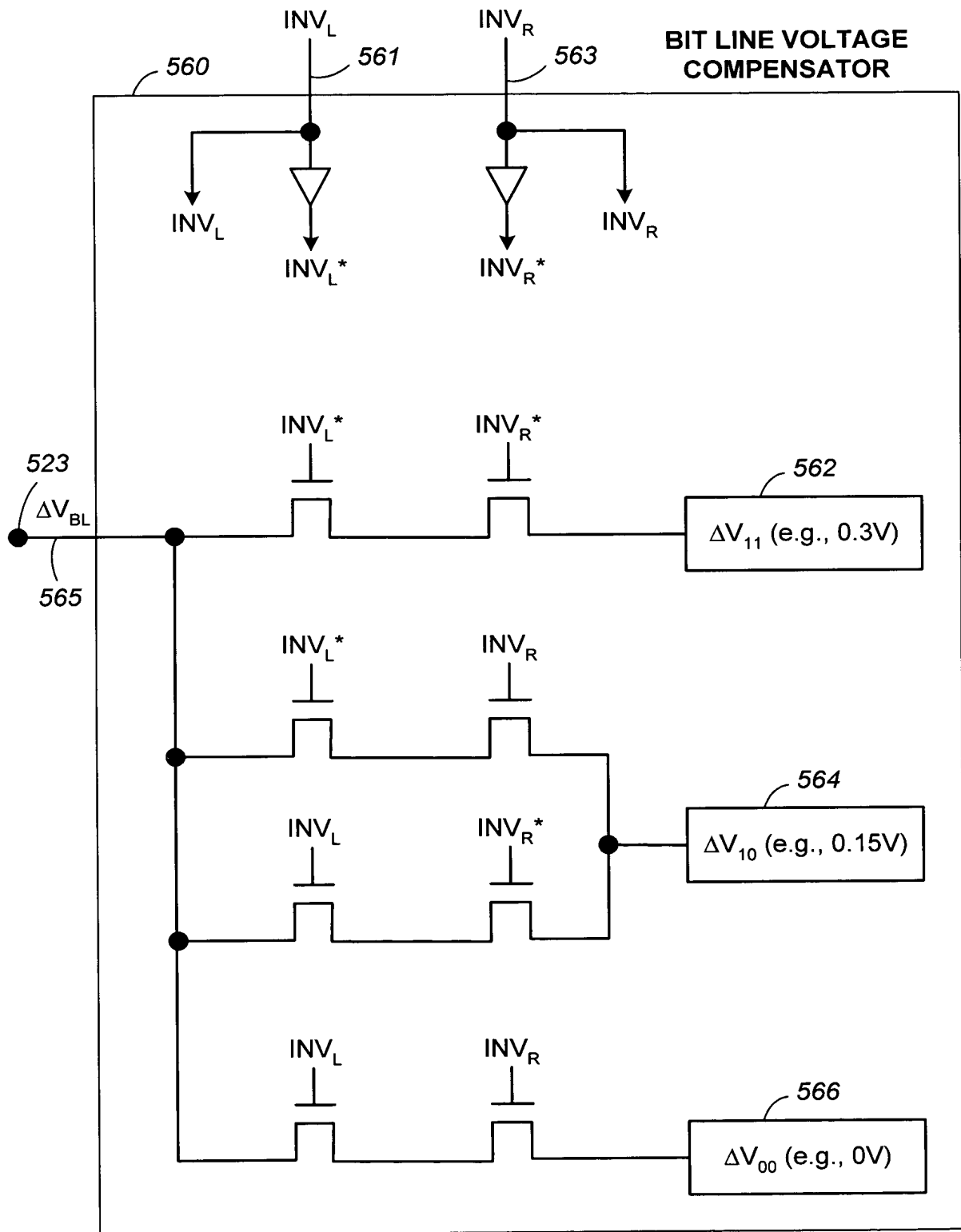


FIG. 12

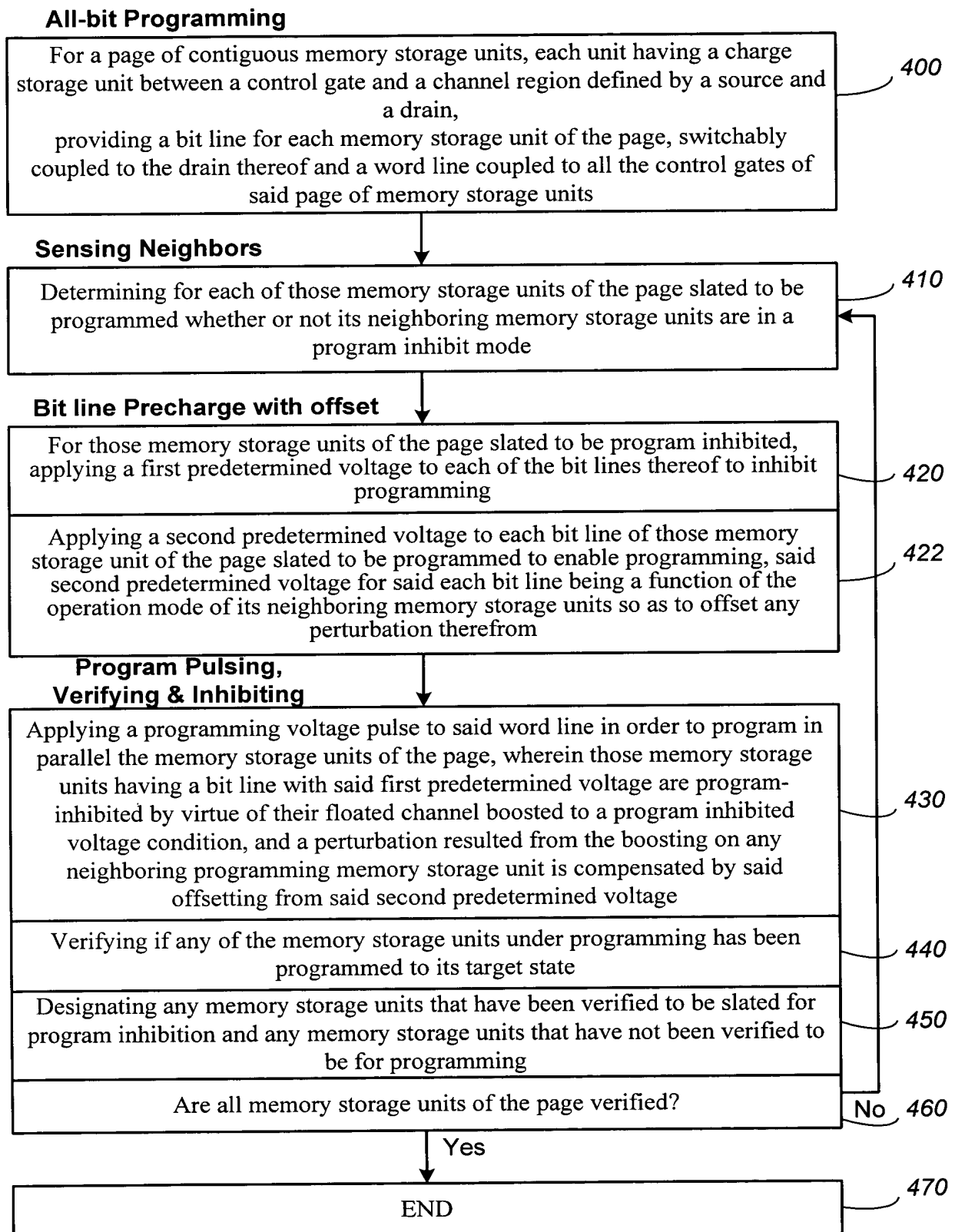


FIG. 13

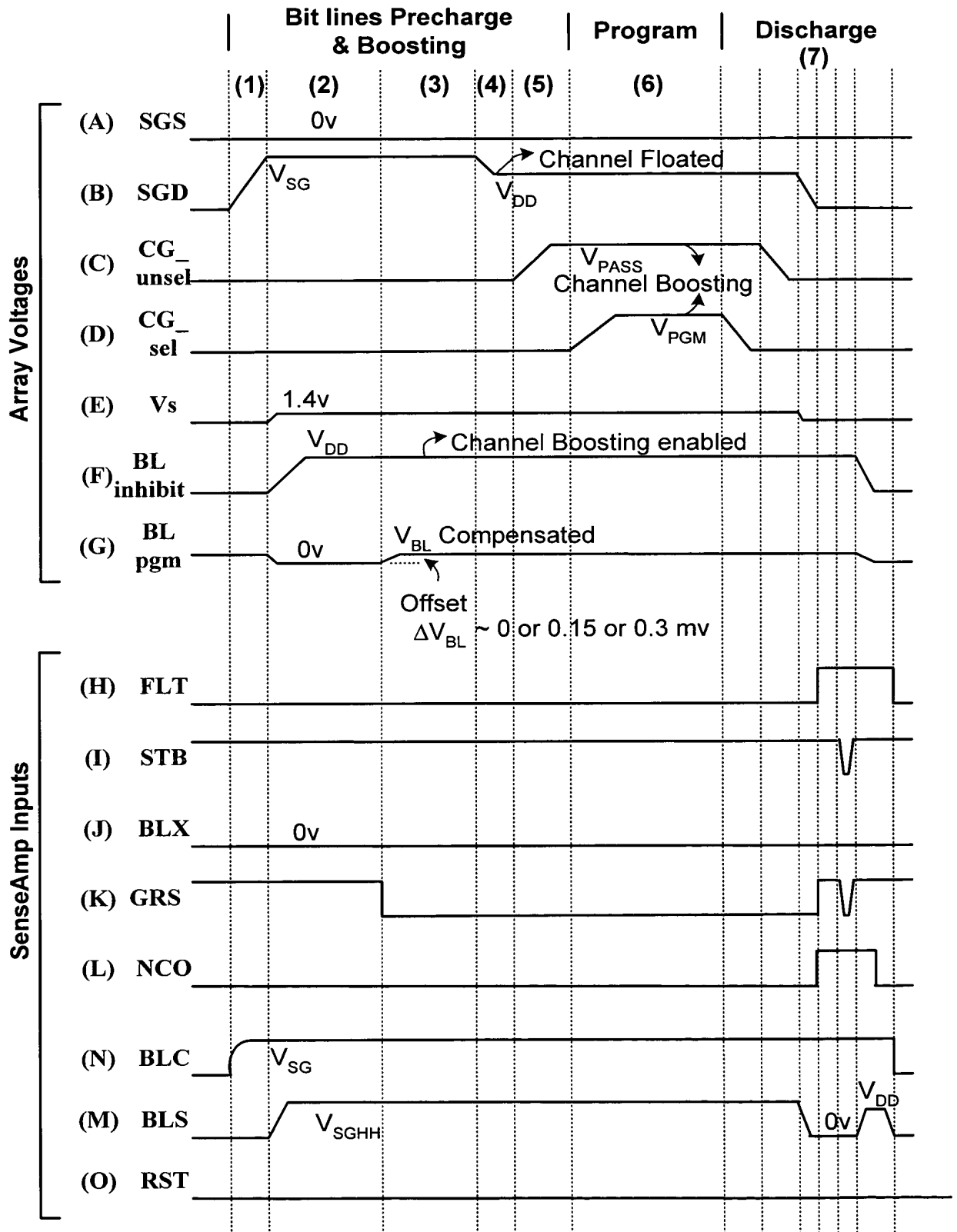


FIG. 14